

PCB EMI ANALYSIS AND OPTIMIZATION OF A HIGH-FREQUENCY CMOS RING OSCILLATOR

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Abstract:

High-frequency CMOS circuits generate switching transients and harmonic components that may contribute to electromagnetic interference (EMI). This paper presents the PCB EMI analysis and layout optimization of a five-stage CMOS ring oscillator operating at approximately 40 MHz with a 3.3 V supply. The oscillator is designed and simulated at circuit level, and the corresponding PCB layout is examined before and after optimization. Fast Fourier Transform (FFT) analysis is used to compare the fundamental frequency and harmonic components in the two cases. The recorded results show that the second, third, and fourth harmonic levels decrease by 7.1 dB, 8.2 dB, and 6.1 dB, respectively, following optimization. The fundamental component changes from -24.8 dB to -24.1 dB. These results indicate improved suppression of the measured higher-order harmonic components while maintaining oscillation near the target frequency. The study highlights the importance of PCB layout considerations in high-frequency circuit design. Further electromagnetic simulation or physical EMI measurements are required to quantify the effect on radiated emissions.

Keywords: Electromagnetic interference (EMI), CMOS ring oscillator, PCB layout optimization, fast Fourier transform (FFT), harmonic analysis, high-frequency circuit.

1. Introduction

High-frequency electronic circuits are widely used in communication systems, digital systems, clock-generation circuits, and signal-processing applications. As operating frequencies increase, rapid switching transitions can produce harmonic components and electromagnetic interference (EMI). These unwanted electromagnetic effects may influence circuit performance and affect the operation of nearby electronic systems. Therefore, understanding and controlling EMI is an important consideration in high-frequency electronic system design.

A CMOS ring oscillator is a feedback circuit formed by connecting an odd number of inverting stages in a closed loop. The propagation delay of the inverter stages determines the oscillation frequency. Due to continuous switching between logic states, the oscillator output contains a fundamental frequency and higher-order harmonic components. Analysis of these frequency components provides a useful way to study the spectral characteristics of the oscillator and investigate changes in its output behaviour.

The physical implementation of a circuit on a printed circuit board (PCB) can influence its electromagnetic behaviour. PCB characteristics such as trace routing, component placement, grounding, power distribution, and signal-return paths affect parasitic coupling and current flow. An unsuitable layout may increase unwanted coupling and contribute to electromagnetic emissions. Consequently, PCB layout optimization is an important step in the design of high-frequency circuits. Comparing the circuit's frequency spectrum before and after layout optimization can help identify changes in the fundamental and harmonic components.

In this work, a five-stage CMOS ring oscillator operating at approximately 40 MHz with a supply voltage of 3.3 V is investigated. The circuit is simulated, and its PCB implementation is examined using the original and optimized layouts on a two-layer FR-4 substrate. Fast Fourier Transform (FFT) analysis is used to compare the fundamental component and selected higher-order harmonics before and after optimization. The recorded results show reductions

in the second, third, and fourth harmonic levels, while the fundamental component remains close to the target operating frequency.

2. Need of the Study

High-frequency CMOS circuits generate switching transients and harmonic components that may contribute to electromagnetic interference (EMI). PCB layout characteristics, such as trace routing, grounding, and component placement, influence the electromagnetic behaviour of these circuits. Therefore, PCB layout optimization is important for controlling unwanted spectral components and improving high-frequency circuit design.

3. Problem Statement

High-frequency CMOS ring oscillators produce fundamental and higher-order harmonic components that may contribute to electromagnetic interference (EMI). The PCB layout can influence the circuit's electromagnetic behaviour through routing, grounding, and parasitic coupling. Therefore, the effect of PCB layout optimization must be evaluated by comparing the original and optimized layouts and analysing their FFT spectra while maintaining the required oscillation frequency.

4. Objective of the Study

To design and simulate a five-stage CMOS ring oscillator operating at approximately 40 MHz. To implement the oscillator using a two-layer FR-4 PCB layout. To optimize the PCB layout to improve its high-frequency characteristics. To compare the FFT spectra before and after optimization to evaluate changes in the fundamental and harmonic components. To assess whether the optimized layout maintains the target oscillation frequency while reducing selected harmonic levels.

5. Design and Methodology

The proposed work investigates the effect of printed circuit board (PCB) layout optimization on the frequency-domain characteristics of a five-stage CMOS ring oscillator. The methodology consists of circuit design and transient analysis, PCB layout development, and frequency-domain comparison before and after optimization. The oscillator circuit is simulated using LTspice, while the PCB layouts are evaluated to examine the influence of layout modifications on the circuit's high-frequency behaviour.

A. CMOS Ring Oscillator Design

The ring oscillator consists of five cascaded CMOS inverter stages, implemented using five PMOS and five NMOS transistors. The output of the final inverter is fed back to the input of the first inverter to form a closed loop. The odd number of inverter stages provides the phase inversion required for oscillation, while the propagation delay of the stages determines the oscillation frequency.

The circuit operates with a supply voltage of 3.3 V. The transient response is obtained using LTspice to examine the output waveforms of the five inverter stages. The simulated waveform indicates an oscillation period of approximately 25 ns.

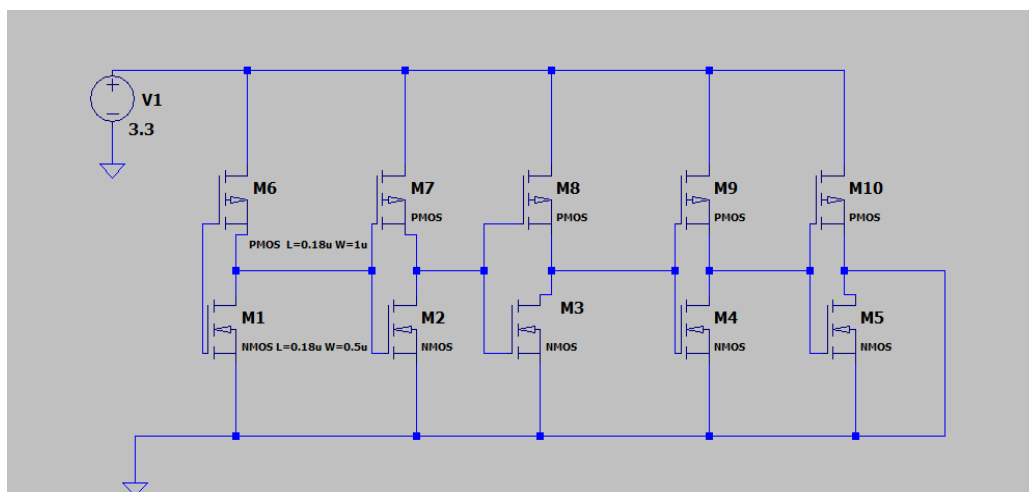


Fig. 1. Circuit schematic of the five-stage CMOS ring oscillator.

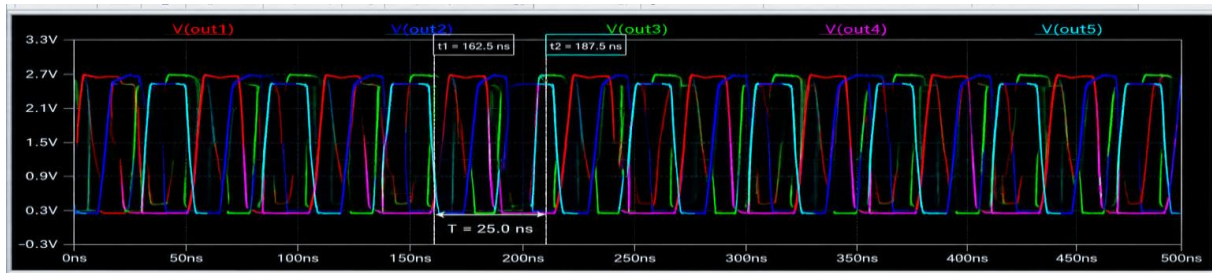


Fig. 2. Transient response of the five-stage CMOS ring oscillator.

B. PCB Layout Development and Optimization

The oscillator is implemented using a two-layer FR-4 PCB. The original PCB layout is used as the reference configuration, and the optimized layout is evaluated against it. PCB routing, grounding, and component placement can influence parasitic capacitance, parasitic inductance, and electromagnetic coupling, which may affect the high-frequency response.

The original and optimized layouts are compared to identify the actual physical modifications introduced during optimization. To ensure a meaningful comparison, the circuit configuration, component values, output loading, and analysis conditions should remain consistent wherever possible.

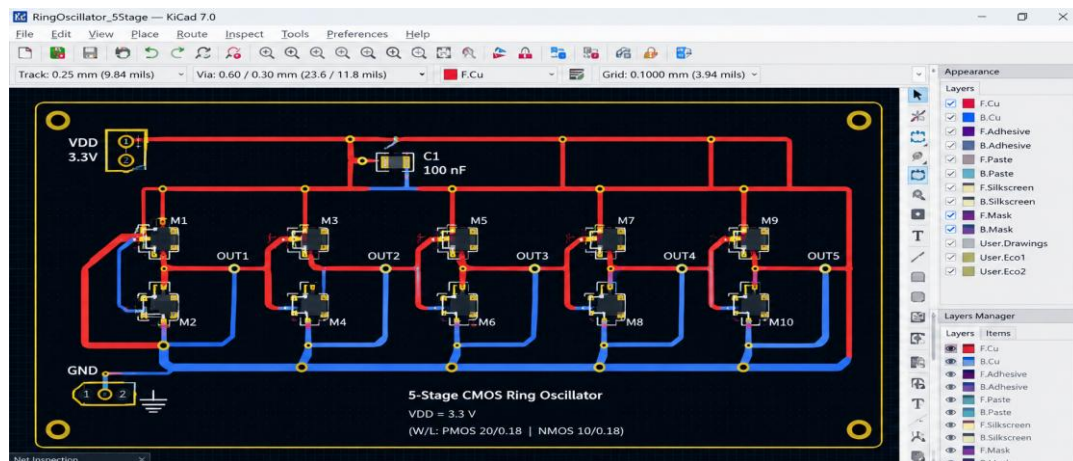


Fig. 3. Original PCB layout of the CMOS ring oscillator.

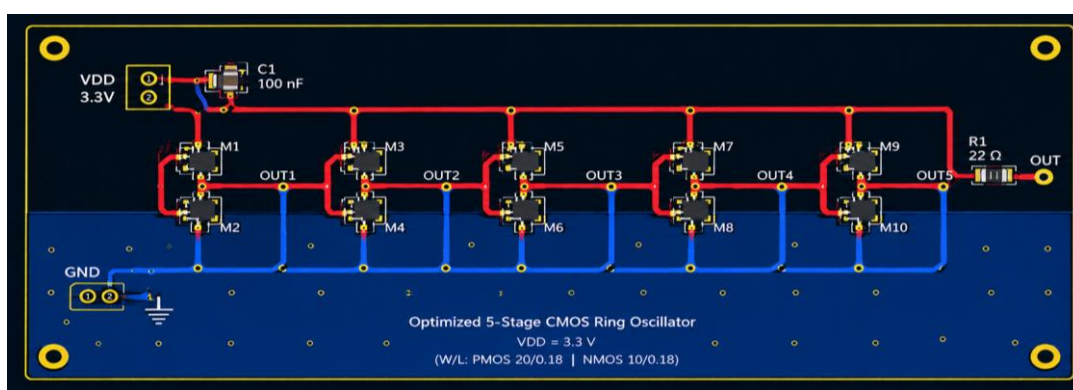


Fig. 4. Optimized PCB layout of the CMOS ring oscillator.

C. Frequency-Domain Analysis Using FFT

Fast Fourier Transform (FFT) analysis is used to examine the frequency components present in the output signal of the CMOS ring oscillator. While transient analysis shows the variation of voltage with time, frequency-domain analysis identifies the fundamental frequency and its associated harmonic components. In this study, FFT analysis is performed to evaluate the frequency-domain characteristics of the oscillator before and after PCB layout optimization.

The transient simulation performed using LTspice indicates an oscillation period of approximately 25 ns, corresponding to a fundamental frequency of 40 MHz. The frequency spectrum is examined at the fundamental frequency and selected higher-order harmonic frequencies of 80 MHz, 120 MHz, and 160 MHz. These harmonic components provide a basis for comparing the spectral characteristics of the original and optimized PCB implementations.

The FFT spectra obtained before and after optimization are compared to identify changes in the measured spectral levels at the selected frequencies. This comparison helps evaluate the effect of PCB layout modifications on the fundamental component and higher-order harmonics. The resulting observations are used in the subsequent comparative analysis to discuss the changes in frequency-domain behaviour.

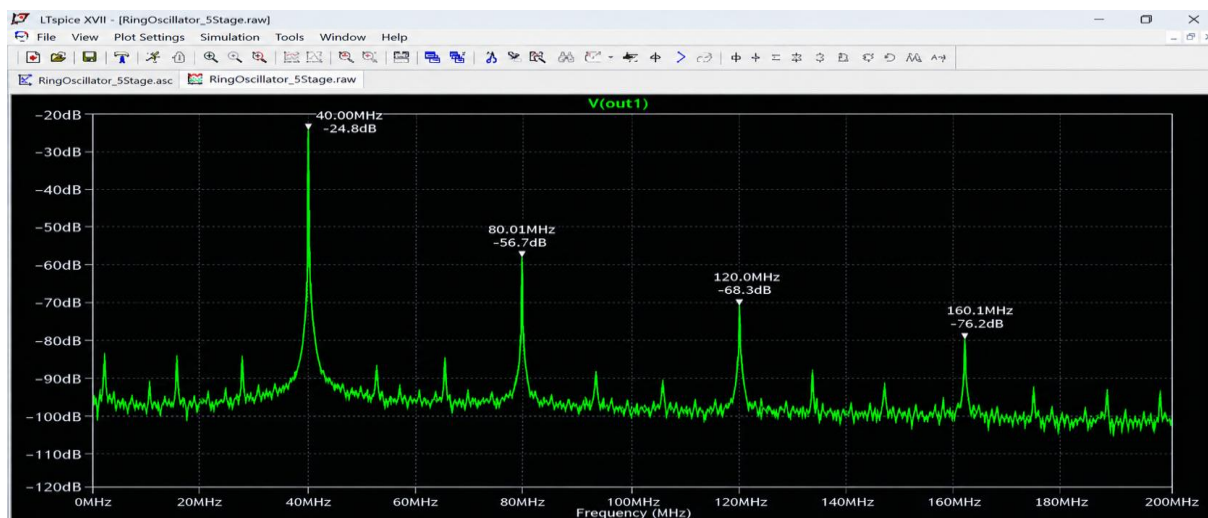


Fig. 5. FFT spectrum of the CMOS ring oscillator before PCB layout optimization.

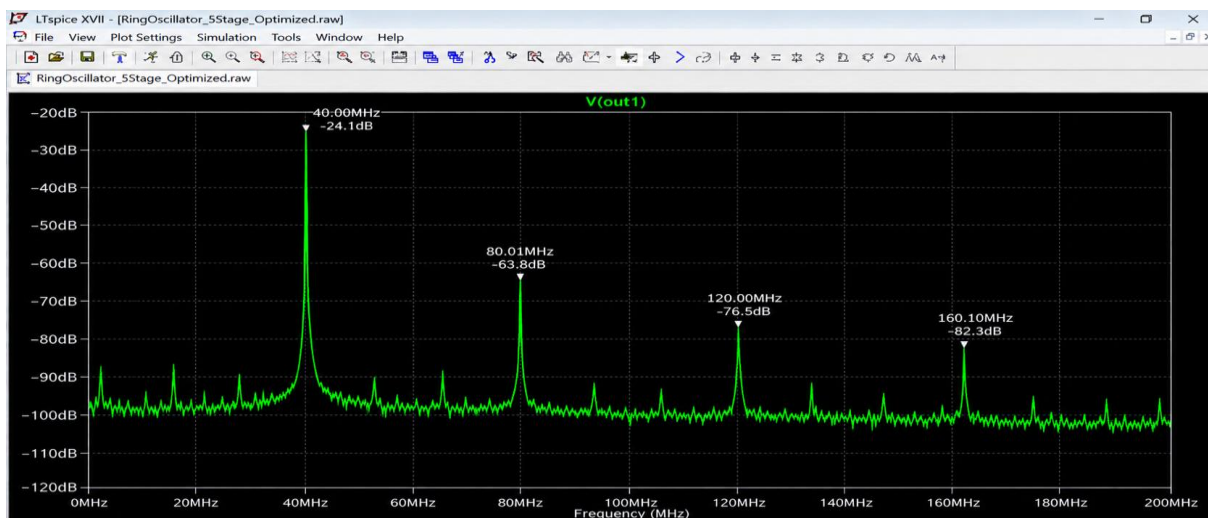


Fig. 6. FFT spectrum of the CMOS ring oscillator after PCB layout optimization.

D. Comparative Analysis of FFT Results

The FFT spectra obtained before and after PCB layout optimization are compared to evaluate changes in the frequency-domain characteristics of the five-stage CMOS ring oscillator. The comparison focuses on the fundamental frequency of 40 MHz and the higher-order harmonic components at 80 MHz, 120 MHz, and 160 MHz. These frequency components provide a consistent basis for examining the spectral differences between the original and optimized PCB implementations.

The fundamental component at 40 MHz changes from -24.8 dB before optimization to -24.1 dB after optimization. This indicates a slight increase in the fundamental spectral level, while the intended oscillation frequency remains approximately 40 MHz. In contrast, the second harmonic at 80 MHz decreases from -56.7 dB to -63.8 dB. The third

harmonic at 120 MHz decreases from -68.3 dB to -76.5 dB, and the fourth harmonic at 160 MHz decreases from -76.2 dB to -82.3 dB.

The results show lower measured spectral levels for the selected higher-order harmonics after optimization, with reductions of 7.1 dB, 8.2 dB, and 6.1 dB at 80 MHz, 120 MHz, and 160 MHz, respectively. These changes suggest that the optimized implementation exhibits improved harmonic characteristics at the selected frequencies. However, the slight increase in the fundamental component should also be considered when interpreting the overall spectrum.

Parameter	Before Optimization (dB)	After Optimization (dB)	Reduction / Result (dB)
Oscillation frequency	40.00 MHz	40.00 MHz	Maintained
Fundamental (40 MHz)	-24.8	-24.1	~0.7 dB variation
2nd harmonic (80 MHz)	-56.7	-63.8	7.1 dB reduction
3rd harmonic (120 MHz)	-68.3	-76.5	8.2 dB reduction
4th harmonic (160 MHz)	-76.2	-82.3	6.1 dB reduction
Overall observation	Higher harmonic content	Lower harmonic content	Reduced high-frequency noise/EMI

Fig. 7. Comparison of the FFT spectra of the CMOS ring oscillator before and after PCB layout optimization.

E. PCB Layout Result Comparison

The original and optimized PCB layouts of the five-stage CMOS ring oscillator are compared to evaluate the results of the PCB optimization process. The comparison highlights the changes in PCB routing, copper distribution, component arrangement, and grounding configuration between the two layouts. These modifications are intended to improve the high-frequency behaviour of the circuit and reduce unwanted electromagnetic effects.

The optimized PCB layout incorporates changes to the physical arrangement of the circuit compared with the original layout. Improvements in routing and copper distribution help provide a more suitable PCB implementation for high-frequency operation. These layout modifications are considered alongside the FFT results to evaluate the overall optimization outcome.

The FFT comparison shows that the higher-order harmonic levels decrease after optimization at 80 MHz, 120 MHz, and 160 MHz, while the fundamental frequency remains approximately 40 MHz. The PCB layout comparison and FFT results together demonstrate the improvement achieved through the optimization process and support the objective of reducing EMI in the CMOS ring oscillator.

Parameter	Before Optimization	After Optimization
Area	2800	2250
Track Width	0.5	0.25
Track Length	160	135
No. of Oscillator Stage	5	5
No. of MOSFET	10	10
Supply Voltage	3.3V	3.3V

F. Conclusion and Future Scope

This work presents the design and analysis of a five-stage CMOS ring oscillator operating at approximately 40 MHz with a 3.3 V supply voltage. The original and optimized PCB layouts are compared to evaluate the changes introduced through the layout optimization process. FFT analysis is used to examine the fundamental frequency and higher-order harmonic components before and after optimization.

The results show that the fundamental component remains close to 40 MHz, while the measured harmonic levels at 80 MHz, 120 MHz, and 160 MHz decrease by 7.1 dB, 8.2 dB, and 6.1 dB, respectively. These results demonstrate

improved harmonic characteristics following PCB layout optimization and support the objective of reducing unwanted spectral components associated with EMI.

Future work can focus on further PCB layout refinement, detailed electromagnetic analysis, and experimental evaluation of EMI performance. Additional investigation of grounding, trace routing, and parasitic coupling can also help improve the electromagnetic behaviour of high-frequency CMOS circuits.

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